Expression (A) gives a dependence of inertial mass of σ as required by Mach's principle and it also give the familiar increase of mass with velocity as obtained in the special theory of relativity, Since, according to Einstein v^2 is of the same order as σ, the neglect of v^2 and retention of σ in Einstein's equation cannot be justified.

But, if we retain the terms which are small of order one compared to the lowest order terms the calculation of "force expression" i.e. the right hand side requires an investigation of the nonlinear terms in the field equatios.

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A NOTE ON DIRECT GENERATION OF PSEUDO RANDOM FREQUENCY SHIFT SEQUENCES

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For testing of transmission networks utilising frequency shift keying it is desirable to have some known deterministic pattern of frequency variation with time. The pattern should have a pseudo-noise character, that is, probability of transition at the end of each bit interval should be one half, as would be expected of a real signal. Utilising such pseudo-random sequences one can measure the expected probability of error and effects of transmission impairments quickly and easily. Pseudo-Random Frequency Shift (PRFS) sequences also find application in N-ary communication system where a particular sequence of M different frequencies corresponds one-to-one to one of N Possible states of the message source.

One way of generating such sequences is to frequency modulate an oscillator with an M-ary PR sequence. In the case of binary ($M = 2$) PR sequences, it is known that such sequences (Golomb 1964, Chakrabarti *et al*, 1966) can be generated by a linear sequential circuit having a cascade of shift registers or digital delay units in combination with a logic circuit consisting of modulo two adders and concidence circuits. An objection to using such a technique is unthat less the amplitude of the binary waveform is very well regulated and the oscillator has a very good stability around its two stationary frequencies of oscilation, the frequency of the output is likely to undergo drift.

A direct method of generating binary PRFS Sequences which avoids the above mentioned difficulty is available. In this method the digital delay unit (refer fig. 1a) consists of a voltage controlled oscillator (VCO) with two continuous inputs at the two state frequencies and a pulsed transfer input at one of the two state frequencies. The amplitudes of these continuous inputs should be small but enough to ensure bistable character of the VCO. The duration of the pulse input should be adequate for causing a transfor of the "state" of the VCO which remains locked with the desired frequency component present in the continuous inputs. Optimum result is obtained by a two mode operation i.e., if the locking range is made larger and the locking time smaller during the transition period. Modulo two adder in the present arrangement consists of a VCO which goes over to state 1 if the two inputs to it are at the same frequency and to state 2 if the frequencies are different. The two inputs (A and B) to the modulo two unit are subtracted from each other and the difference output is detected. The detected output is fed to a switching device to obtain bipolar input to C (refer fig. 1b). Initial conditions or states of the VCO are set by applying d.c. voltages of appropriate polarities to the VCO. This technique of generation of PRFS sequence will ensure a good degree of frequency and phase stability within the individual bits constituting the sequence.

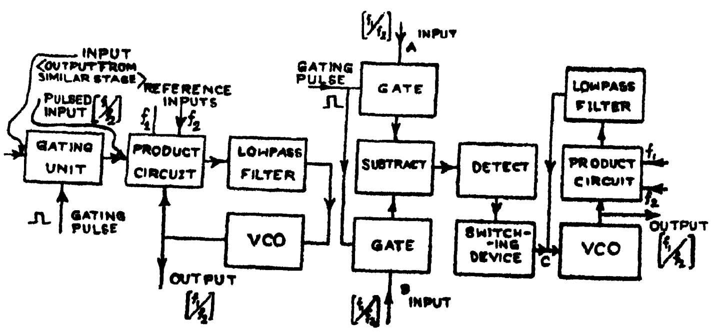

Fig. 1(a) Fig. 1(b)

Block representation of a typical r. f. digital delay unit is shown in fig. 1(a) and that of a module two unit is shown in fig. 1(b).

To assure a good degree of stability it is necessary to derive the reference frequencies (f_1 and f_2) from stable sources or from a single source following coherent generation techniques which may be categorised as *i*) sideband selection, ii) controlled scaling, iii) feed forward and iv) feed back type. A crystal controlled r.f. oscillator is used as the reference source in all such systems. In sideband selection type the desired frequencies (f_1 and f_2) are derived from the reference one (f_0) using a chain of divider and a balanced modulator. In the method referred to as controlled scaling the internal logic of the scaling unit is such that output pulses having repetition frequencies f_1 and f_2 are obtained using the reference source as a clock pulse generator. The pulses are made to pass through filters centred at f_1 and f_2 to produce the continuous signals. In the feed forward type, the pulse train fro the clock pulse generator is fed in parallel to a divider and a scaling unit. A controlled number of output pulses from the divider is also applied (fed forward) to the scaler. In the feed back type, the incoming pulse train is fed to a scaling unit and from the scaler a controlled number of pulses obtained is fed back (in parallel with the incoming pulse train) to the scaler.

The switching signal controlling the bit timing can also be derived from the stable local source by the process of frequency division. Thereby the switching instants are determined *a*-priori. The bit period is chosen so as to accomodate an integral number of r.f. cycles irrespective of the state of the particular bit within the sequence. The instant for change over is chosen such that the transient generated in swit ching is a minmum.

For generation of multilevel sequences one can obviously make use of the same type of shift register having required number of reference states at its inputs and stationary states. The modulo *M* adder is more difficult to realise. One method is to detect the frequencies of the inputs to the adder and use these to obtain modulo *M* output by means of a video adder. The output of the modulo *M* adder then controls the state frequencies to be gated to the VCO.

For the ternary case one alternative realisation of the modulo three adder could be as follows. If the frequencies of the two inputs are identical the frequency of the output would be $2f_o - f_n$. If they are different the output would be $f_1+f_2-f_0$; where f_0 is the arithmetic mean of the three state frequencies (f_1, f_0 and f_2) i.e., $f_1-f_0 = f_0-f_2$.

It should be mentioned that multipath phenomenon (where a number of signals suffering different amounts of time delays arrive at a receiving point) can be easily simulated using the above type of r.f. digital delay units. To obtain any required time shift one has only to delay the gating pulse by the appropriate amount.

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